# RAM (VHDL)



## Code Download

ram.vhd

## Features

- VHDL source code of a single port RAM component
- Configurable memory size
- Configurable width of each data word
- Synthesizes into the internal memory block resources of most FPGAs

## Introduction

This details a single port RAM circuit, written in VHDL. This memory component outputs data from the memory address specified and also writes input data to this address if a write enable is asserted. It was designed using Quartus Prime, version 17.0.0. Resource requirements depend on the implementation. Figure 1 illustrates a typical example of the RAM integrated into a system.

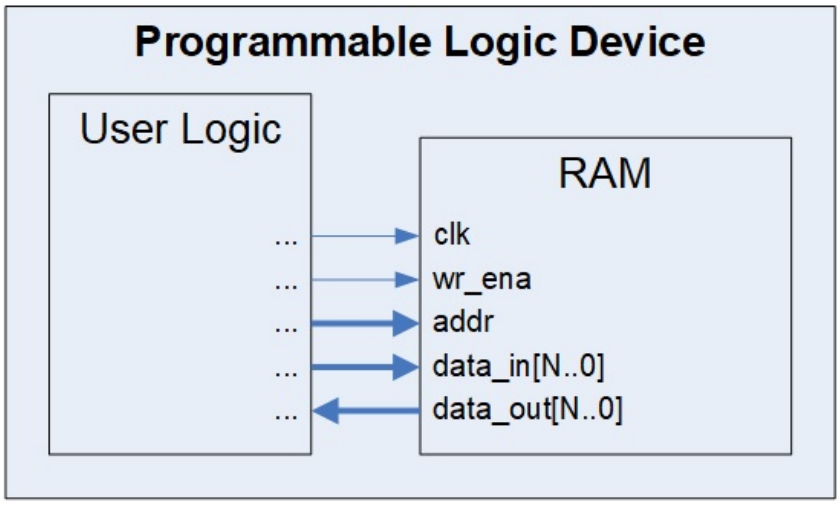


**Figure 1.** Example Implementation

## Architecture

This RAM uses a write-before-read architecture. During a write cycle, the RAM writes the data before reading it on the output port, so the data shown on the output port is the same as that being written, rather than the old data that is being overwritten.

## Configuring the RAM

The RAM is configured by setting the GENERIC parameters in the ENTITY. Table 1 describes the parameters.

**Table 1.** Generic Descriptions

| Generic | Data Type | Default | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| d_width | integer | 8 | The width of each data word |
| size | integer | 64 | The number of data words the memory can store |

# Port Descriptions

Table 2 describes the RAM's ports.

**Table 2.** Port Descriptions

| Port | Width | Mode | Data Type | Interface | Description |
|---|---|---|---|---|---|
| clk | 1 | in | standard logic | user logic | System clock |
| wr_ena | 1 | in | standard logic | user logic | Write enable: synchronously writes data on *data_in* port to the memory location specified on *addr* port when '1' |
| addr | M^ | in | integer | user logic | Address of memory location to access |
| data_in | N* | in | standard logic vector | user logic | Data to be written to memory location *addr* if *wr_ena* is asserted |
| data_out | N* | out | standard logic vector | user logic | Data currently stored in memory location *addr* |

Notes
* N is the specified width of a data word, set by the *d_width* generic in the entity
^ M is the required width for an integer equal to the memory size, set by the *size* generic in the entity

# Conclusion

This programmable logic RAM is a simple, single port memory component that outputs data from the specified memory address and, if a write enable is asserted, writes input data to this address. The number of memory locations and the data width are both configurable.

# Contact

Comments, feedback, and questions can be sent to eewiki@digikey.com.