A KYOCERA GROUP COMPANY

One AVX Boulevard
Fountain Inn, SC 296644

Aging and Other Factors that Affect MLCC Capacitance Measurements

The capacitance value of multilayer ceramic capacitors can be affected by several factors, including temperature, voltage, frequency, and time. These characteristics are well known and consideration for them is generally incorporated into circuit design and component selection. AVX and other MLCC manufacturers also consider these factors when setting the limits for 100% capacitance testing that is done during the manufacturing process. There are also cases where circuit assemblers will need to consider these factors. ANSI/EIA-521 "Application Guide for Multilayer Ceramic Capacitors- Electrical" is a good reference for this subject. The AVX catalog also includes information on factors that can affect the measured capacitance value.

Users should know that AVX capacitors are 100% tested for capacitance value in our manufacturing process using precision capacitance meters. The testing is validated by QC sampling. We are confident that our products have the correct capacitance values, but the information below may be helpful in cases where the measured capacitance value is not within the expected range.

Measuring Capacitance

Measurements should be made using a precision capacitance meter and the measurement conditions shown in the table below. Measurements made using other ac conditions or dc techniques may not be suitable for judging whether the capacitors are within specification. A meter with Automatic Level Control function may be needed to maintain the desired test voltage for capacitance values ≥ 1 µF, and the ALC function must be turned ON. Without ALC the measurement voltage can drop due to high measurement current. This can cause a significant reduction in the measured capacitance values.

Category	Measurement Voltage	Measurement Frequency
Class I (NPO/COG), C ≤ 1000 pF	1.0 Vrms	1.0 MHz
Class I (NPO/COG), C > 1000 pF	1.0 Vrms	1.0 kHz
Class II (X7R, X5R, etc.) C ≤ 10 µF	1.0 Vrms	1.0 kHz
Class II (X7R, X5R, etc.) C > 10 µF	0.5 Vrms	120 Hz

Aging in Multilayer Ceramic Capacitors

"Aging" in ceramic capacitors is a gradual decrease in capacitance over time. This phenomenon is common to all Class II and Class III ceramic capacitors, including BX, X8R, X7R, X7S, X5R, and Y5V types, regardless of the manufacturer. Class I (NPO / COG) capacitors are "non-aging".

The aging cycle begins when ceramic capacitors are heated to 125°C or higher. In our manufacturing process this occurs when the capacitors are baked near the end of the manufacturing sequence. This is referred to as "deaging"- it resets the crystal structure of the ceramic dielectric material to a higher energy state. Deaging also occurs during during circuit assembly when the capacitors are soldered to the pcb.

The measured capacitance value is higher after deaging. Realignment to the lower energy state occurs gradually, and the capacitance gradually returns to its steady state value. This is the aging effect, and the capacitance change is linear versus log time.

Effects of Aging

The customer may see the aging effect in two ways.

1. The capacitance value of unused parts from the reel may be lower than expected due to aging. This will be corrected during circuit assembly when the capacitors are soldered to the pcb. Or, bake the sample at 150°C for one hour, then wait 24 hours- the capacitance value will be restored to the deaged condition.

2. The capacitance value after soldering may be higher than expected. This is a temporary condition that is more likely to be observed within the first 48 hours after soldering. The higher values may result in out-of-tolerance rejections at ICT. Our recommendation in these cases is to adjust the ICT test limits as needed to accommodate the temporarily higher capacitance values. The capacitance will revert to the steady state value and typically will be within tolerance after 48 hours (some PN's may take longer).