Replacing Cypress CY14B101LA nvSRAM with Everspin MR0A08B MRAM

Low Cost, High Reliability, and Unlimited Endurance with Everspin MRAM

Application Note EST-1010 provides the necessary information to replace the Cypress CY14B101LA with low cost, highly reliable, and unlimited endurance Everspin MR0A08B.

Everspin Non-Volatile Memory
Everspin is the global leader in MRAM technology. Our award-winning MRAM product family is in high volume production. The MR0A08B is a 1Mb member of the MRAM family organized 128Kx8.

Highly Reliable, Non-Volatile Data Storage
Every write with MRAM is instantly non-volatile. There is no transfer of data from volatile to a non-volatile memory cell after power failure. Everspin MRAM requires no external capacitor to enable its nonvolatility. MR0A08B power cycling is simpler and more reliable than nvSRAM.

Data written in MRAM will be retained for a minimum of 20-years and is retained independent of the number of read/write and power cycles.

Compatibility
The Everspin 1Mb MRAM MR0A08B is pin and timing compatible with the Cypress 1Mb nvSRAM CY14B104L. MR0A08B does not require an external capacitor and other passive components needed by the CY14B104L.

Everspin MRAM allows the system designer to take advantage of a less complex, more reliable non-volatile solution by saving board area, reducing cost and simplifying design.

The Everspin 1Mb MRAM MR0A08B is available in 44-pin TSOPII and 48-pin BGA packages.

Benefits of MR0A08B
The Everspin MRAM solution provides:

- Cost Effective Board Design
- 20-Year Data Retention with No Cycling Dependence
- Always Non-Volatile – No Unreliable Capacitor Dependent Backup Cycles
- No Wear-out Concerns

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A capacitor is normally connected on nvSRAM boards between the V<sub>CAP</sub> pin and ground. Everspin assigns a don't connect to the corresponding pin 30 (TSOP II) and ball E3 (BGA). These should be either ground or floating. The capacitor will have no effect on MRAM operation. The /HSB pin 44 of the nvSRAM may be unconnected or potentially pulled up to V<sub>DD</sub> or V<sub>CAP</sub>. The MRAM does not connect assigned to pin 44 (TSOPII) is not affected by a logic high signal. The equivalent MR0A08B ball, G2 is a no connect and is not affected as well.

If properly connected, MRAM directly replaces nvSRAM.

**MRAM Provides Compatible Timing to nvSRAM**

Both Everspin MRAM and nvSRAM have standard asynchronous SRAM timing. The MRAM operates with a 35 ns read/write cycle time and is compatible with similar nvSRAM speed grade options.

All major address, data, control, and power supply pins are identical between nvSRAM and MRAM. The primary differences are two pins on the nvSRAM (V<sub>CAP</sub> and /HSB). These functions are not required for operation of the MRAM and are used to support the nvSRAM backup cycle.
Simplified Power Cycling Considerations

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period. When power fails, Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

The nvSRAM part needs the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. This raises concerns about reliability of the backup storage cycle under all system power conditions including some that cannot easily be simulated or tested.

There may be concern with wear-out of nvSRAM EEPROM storage element which is limited to just 200K cycles. Everspin MRAM supports unlimited read, write, and power cycles. There are no wear-out concerns with MROA08B.

Power Supply Considerations

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents. Use proper decoupling capacitor to assure reliable operation.

Reliability Considerations

CY14B101LA uses conventional trapped charge technology for non-volatile storage. Data can leak away as a result of temperature and damage from write cycles. Data retention time is dependent on the number of write cycles. This currently limits nvSRAM to industrial temperature operation. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 200K cycles.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external $V_{cap}$ capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125 °C. The MROA08B will be offered in automotive temperature range in the near future.

Efficient Cell Design

Everspin MRAM will provide the most cost effective non-volatile RAM solution. nvSRAM is constructed by combining both a standard 6-transistor SRAM and an EEPROM non-volatile storage element in every cell. The total cell complexity is 12-transistors. MROA08B is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency.
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